

LGIT CSP Application NOTE

(Lighting)



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1. LGIT CSP Details

1.1 Description

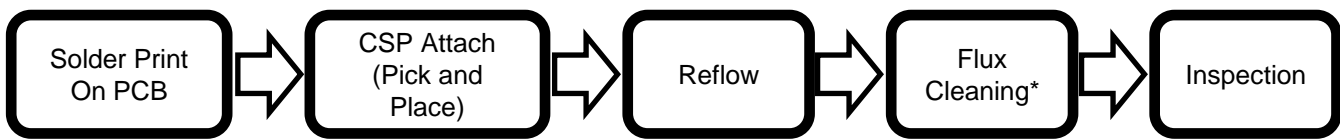
. For usage, LGIT CSP needs to be mounted on PCB with SMT process. (Fig.1)

. LGIT CSP 's top and sides consist of a mixture of Phosphor and Silicone. (Fig.2)

Chip pads are exposed on the lower side of CSP and the pads consist of gold.

. Cathode pad includes notch mark. (Fig.3)

Cathode mark is not limited by the marked area from the Fig.3 (marked area is an example).



* Flux Cleaning Process will be added when customer requests.

Fig. 1. SMT process flow

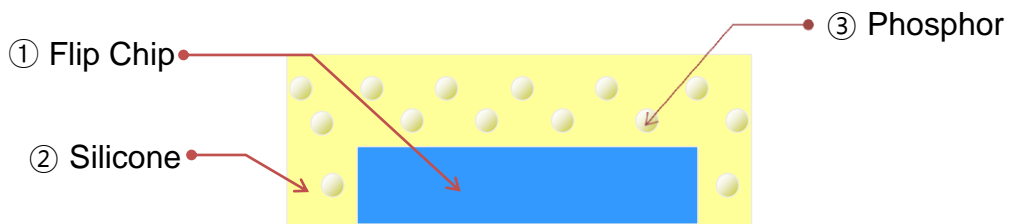


Fig. 2. CSP Structure

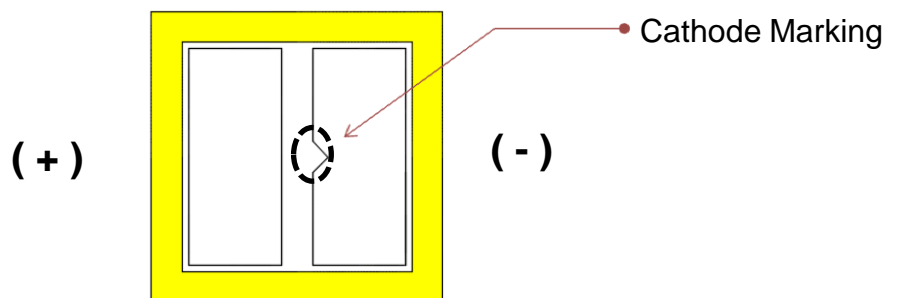


Fig. 3. Anode and Cathode markings

2. LGIT CSP Printed Circuit Board (PCB) Design

2.1. LGIT CSP Footprint and PCB Pattern

. Bottom side of LGIT CSP includes two pads types.

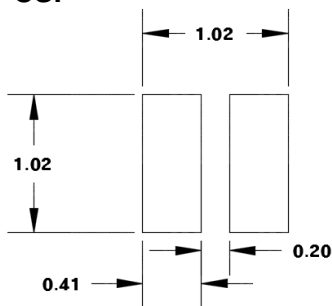
And pattern designs of Fig. 4 and 5 are recommended for safe electrical operation and efficient heat release. (Fig. 4, 5)

E.g.) LGIT CSP 1515, 1919

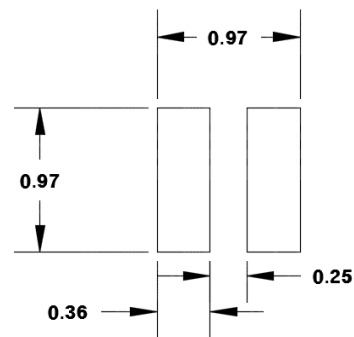
◆ **Recommendable soldering pattern**
(Solder type : SAC 305 type6 or 7)

◆ **Recommendable Stencil Design**
(Stencil depth : 0.1mm)

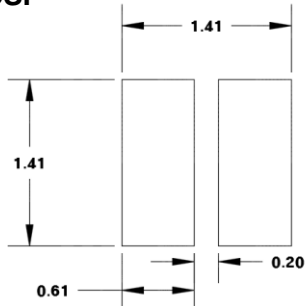
1515 CSP



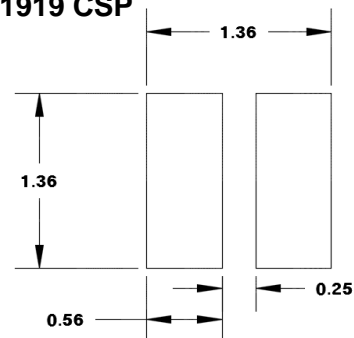
1515 CSP



1919 CSP



1919 CSP



*All dimensions in mm

Fig. 4. Recommended CSP Footprint and PCB Pattern

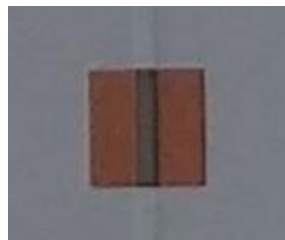


Fig. 5. Actual PCB footprint

2.2. PCB Substrate Selection

. The characteristics for each PCB type. (Table. 1)

	FR4	MCPCB	Ceramic PCB
COST	low ~ medium	medium	high
Coefficient of thermal expansion (CTE)	Good	Moderate	Good
LED assembly packing density	Low density applications	Medium density applications	High density applications
Mechanical assembly & handling	Easy as board does not easily break	Easy as board does not easily break	Hard & Brittle

2.3. Surface finishing on Copper

. In case of PCB which has small pad and pitch, it is recommended to use the electro-less nickel immersion gold (ENIG) or organic solder-ability preservative (OSP) over copper pad.

2.4. Silk Screen or Ink Printing

. It is not recommended to indicate any marks around CSP.

If it is needed, the marks should be apart from CSP over 1mm.

2.5. PCB mask (Stencil) Deviation

. Mask Deviation should be managed within $\pm 50\mu\text{m}$. (Fig.6)



Fig. 6.

- * 1. PSR in color is recommended to be white due to CSP's own characteristics.
- 2. PSR's reflectivity is recommended to be above 80%.

3. LGIT CSP Assembly Process

. SMT process is indicated briefly as Fig. 1.

3.1. Solder Paste

. For LGIT CSP, It is recommended to use SAC305 solder paste (96.5% tin, 3% silver and 0.5% copper) type 6 or 7 (Maker : Alpha Advanced Materials).

* Caution: Need to be careful the ESD when the process is on going.

3.2. Mask Print (Stencil Printing)

It is recommended to use the mask that has 100um thickness.

Recommended mask conditions are:

1. An opening should have uniform thickness and be without particles or dust
2. To minimize the deviation between mask and PCB to prevent leakage of solder cream from foot print.
3. To use recommended mask size on Fig. 4.
4. To use workstation which is suitable to mechanically support PCB on the printing process (Fig. 7)

Auto : need to be marked "Fiducial" at Mask and PCB to improve the degree of precision.

Manual : Not suitable for the chip scale PKG.

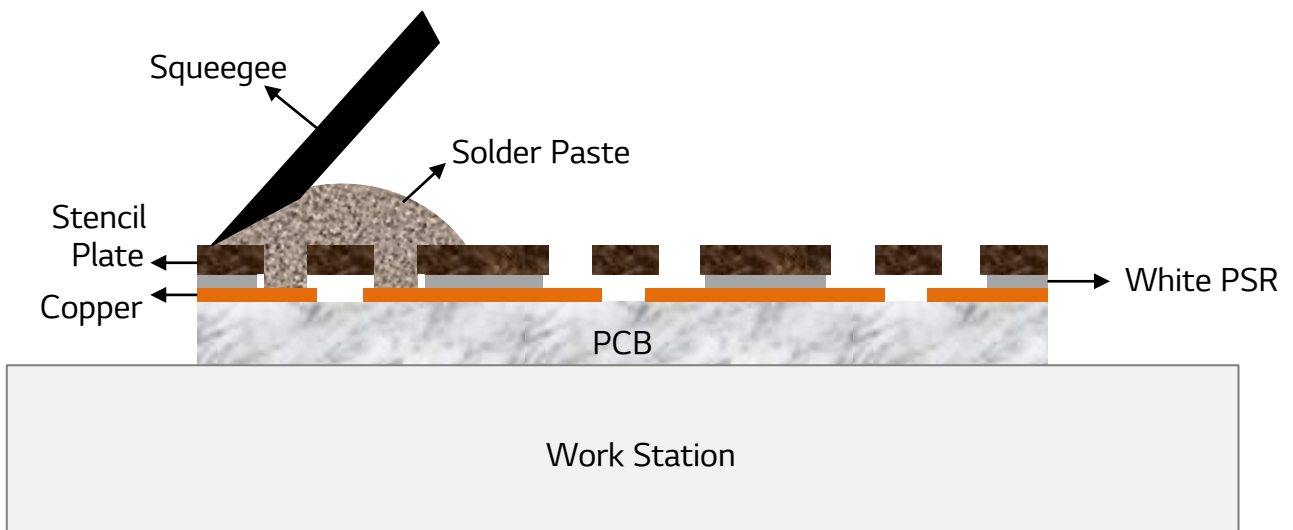


Fig. 7 Auto stencil printing Machine

3.3. Pick and Place

100um of thickness of mask is recommended to be used.

1. Selection of the Collet

- It is recommended to use Teflon type collet to prevent the sticky issue on CSP surface.
- Recommended Collet size (In case of Square type CSP)
 - . Internal diameter (ID) : CSP size x 0.55
 - . Outside diameter (OD) : CSPsize x 0.85
- Collet surface should be very clean without any dust and broken surfaces.

2. Selection of Eject Pin

Recommended Pins to maximize the efficiency and minimize the damage is:

- Material type : Teflon
- R : 100um (Depending on CSP size)
- Maker : Sungjin Tech in Korea (MS-7C-L17A20R150-P)
- ※ It is not recommended to use the Tungsten type pin to prevent damage on back side of chip.
- ※ Above recommended conditions could be changed according to test conditions.

Fig. 8. Recommend Collet Z mount value and the condition to prevent the electrical short

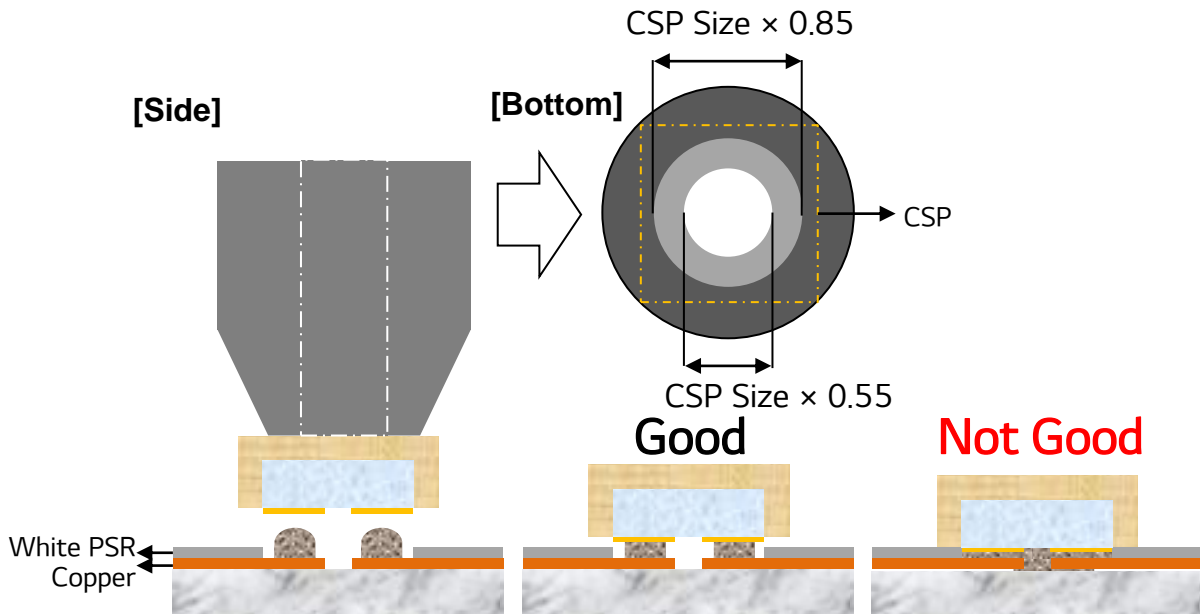


Fig. 8. Left : Pick up image (ID and OD is same as recommend)

Middle : Optimized Height condition (OK)

Right : Short would be expected after reflow process due to immoderate Z mount value.

3.4. Pattern Recognition

It is recommended to recognize each small pads of chips, not CSP's outside size to have right position on PCB.

3.5. Reflow

Recommended reflow conditions

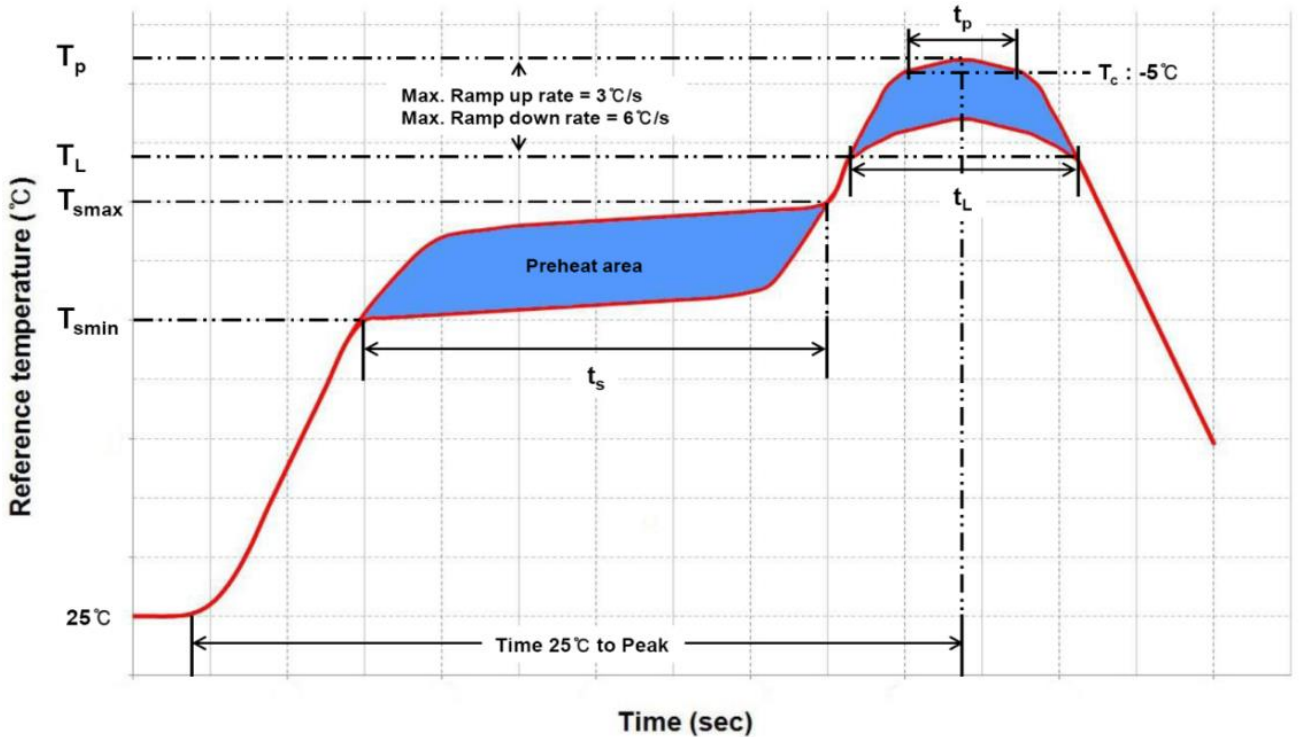


Fig. 9. Solder reflow profile

Table. 2

Profile Feature	Pb-Free Assembly	Pb-Based Assembly
Preheat/Soak Temperature Min(T_{smin}) Temperature Max(T_{smax}) Maximum time(t_s) from T_{smin} to T_{smax}	150°C 200°C 60~120 seconds	100°C 150°C 60~120 seconds
Ramp-up rate (T_L to T_p)	3°C/ second max.	3°C/ second max.
Liquidous temperature (T_L)	217°C	183°C
Time (t_L) maintained above T_L	60~150 seconds	60~150 seconds
Maximum peak package body temperature (T_p)	260°C	235°C
Time(t_p) within 5°C of the specified temperature (T_c)	30 seconds	20 seconds
Ramp-down rate (T_p to T_L)	6°C/second max.	6°C/second max.
Maximum Time 25°C to peak temperature	8minutes max.	6minutes max.

3.6. Flux Cleaning

It is highly important to eliminate “Flux” from PCB surfaces after reflow.

“Flux Cleaning” allows to secure effective performance and reliability data of CSP.

<Cleaning Condition>

1. To proceed after having ESD protection condition
2. To heat DI (Deionized) water and De-flux cleaning solution up to 60°C in a vessel
3. To sink reflow-finished CSP into the vessel, and to proceed cleaning with Ultrasonic for about 5 minutes
4. To wash cleaned CSP in running DI water for 3 minutes
5. To look at CSP with microscope if it would be perfectly finished after flux cleaning
6. If it would be finished perfectly, to move onto next process, or not, perform cleaning repeatedly
7. To bake CSP at 80°C for 5hours to remove moisture

3.7. Electrostatic Discharge Protection

LGIT CSP is guaranteed up to ESD 2kV referring to JEDEC standard (Document : JESD625B)

“Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices”

- To use board designed in accordance with JESD625B for working
- During working, to wear protective equipment which prevents ESD (e.g.: Wrist Straps)
- During CSP’s storage and handling, to remove static and/or particles on the surface of CSP (e.g. : Usage of Ion Blower)
- To store CSP in a bag which is anti-ESD

※ Above is general conditions for ESD protection, and additional protection could be needed depends on the product application.

4. Caution for Manual Handling

In principle, CSP itself should not be touched with tweezers.

In unavoidable case, Anti electrostatic tweezers should be used for manual handling.

To hold sides of CSP with tweezers and not to touch upper side of CSP (Fig. 10)

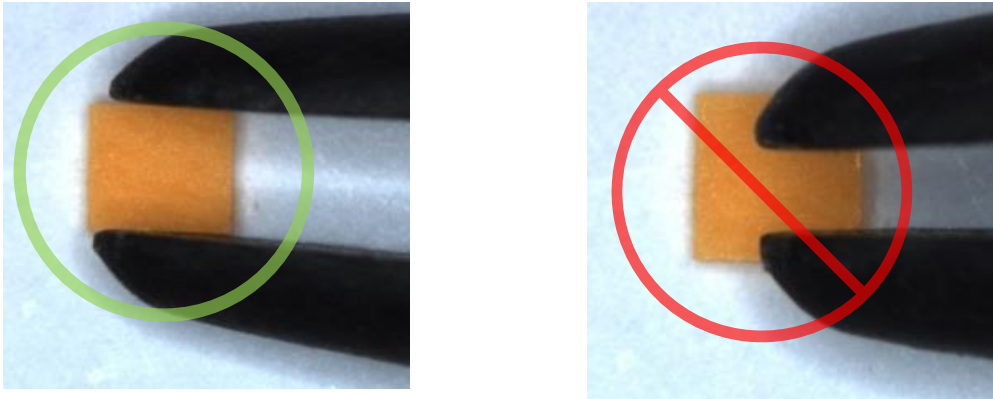


Fig. 10.

